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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,576	08/05/2003	John M. MacLaren	200301722-2	6985

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EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,576	MACLAREN ET AL.	
	Examiner	Art Unit	
	Paul A Baker	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *2 and 11-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10 and 16-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/05/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 5 August 2003 has been entered.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 2-5, 8 and 9 of US Patent 6,640,282 contain every element of claims 1, 3-5, 9 and 10 of the instant application and as such anticipate claims 1, 3-5, 9 and 10 of the instant application.

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claim 6 is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 5 of prior U.S. Patent No. 6,640,282 ('282). This is a double patenting rejection. Claim 5 of '282 was rejected under 35 USC §112 2nd paragraph. The position of the examiner is that the limitations presented in claim 3 are superceded by the limitations of claim 5. Therefore claim 6, while dependent upon claim 3, does not contain the limitations presented in claim 3. Therefore the double patenting rejection of claim 6 is statutory.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Santeler US Patent 6,223,301.

In regards to claim 1, Santeller discloses powering-up a segment of semiconductor memory in a computer system, comprising the acts of

inserting the segment of semiconductor memory into the computer system while the computer system is operating in column 5 lines 61-63;

initializing the segment of semiconductor memory while the computer system is operating is inherent to a hot-swappable memory system;

rebuilding the segment of semiconductor memory while the computer system is operating in column 5 lines 56-60; and

verifying the segment of semiconductor memory for validity while the computer system is operating in column 5 lines 41-49.

Santeler does not disclose the segment of semiconductor memory comprises a memory cartridge. Santeler discloses the memory segment to be a memory module. The use of memory modules or memory cartridges is nearly always interchangeable in the design of memory subsystems. The replacement of Santeler's memory modules with memory cartridges would yield the same functional system. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute Santeler's memory modules with memory cartridges.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Santeler US Patent 6,223,301 in further view of Bellamy US Patent 5,268,592.

In regards to claim 3, Santeler does not disclose sequentially connecting a plurality of pins at an interface, the interface comprising a connector configured to couple the memory cartridge to the computer system in response memory cartridge being inserted into the computer system; and sequentially enabling a plurality of signals in response to the sequential connection of the plurality of pins.

Bellamy discloses sequentially connecting a plurality of pins, sequentially enabling a plurality of signals in response to the sequential connection of the plurality of pins. While Bellamy is not specifically disclosed for computer memory cartridges being inserted, Bellamy discloses hot-plugging cards into a computer board of which computer memory subsystems are a subset. In addition Santeler discloses the desire for hot-pluggable memory in column 5 lines 60-63, Bellamy discloses a method of eliminating damage to the computer card and board when hot plugging cards into the system. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to sequentially enabling a plurality of signals for the purpose of safely inserting memory into a system which is powered up.

In regards to claim 4, Bellamy discloses the plurality of pins comprise varying pin lengths, the pin lengths assigned to sequentially connect the plurality of pins upon insertion memory cartridge into the computer system in figure 1 element 18.

Claim 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Santeler et al. US Patent 6,223,301 in view of Olarig et al. US Patent 6,098,132.

In regards to claim 5, Santeler does not disclose act (a) comprises:

connecting one or more ground pins from the memory cartridge to the computer system;

connecting one or more power pins from the memory cartridge to the computer system;

connecting one or more first insertion removal sense pins from the memory cartridge to the computer system;

connecting one or more data pins from the memory cartridge to the computer system; and

connecting one or more second insertion removal sense pins from the memory cartridge to the computer system.

Olarig inherently discloses connecting one or more ground pins from the memory cartridge to the computer system, connecting one or more power pins in figure 3 PWRON bubble, connecting one or more first insertion removal sense in column 22 status table bit 24, connecting one or more data pins in figure 3 BUSON bubble, connecting one or more second insertion removal sense pins in column 22 status table bit 16. Olarig discloses the benefits of incorporating of redundant memory in column 14 lines 53-59. Likewise Santeler discloses the benefits of incorporating his invention with

hot swap memory modules in column 2 lines 24 – 28. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate connecting pins to facilitate safely inserting a memory cartridge into the memory sockets when the system is operating.

In regards to claim 10, Santeler does not disclose act (a) comprises the act of locking the memory cartridge into the memory system. Olarig discloses locking the memory cartridge in place with a solenoid in column 2 lines 43-49.

Claims 16-19, 25-27, 29-30, 32, 37, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. US Patent 6,098,132 in view of Santeler et al. US Patent 6,223,301.

In regards to claim 16, Olarig discloses a computer system comprising a host controller in figure 9 element 318, a memory sub-system coupled to the host controller, the memory sub-system comprising:

a memory system board in figure 9 element 320, the memory system board comprising an indicator configured to notify of user of errors in the memory sub-system in figure 5 elements CRERR, UCERR, and INTR#;

a plurality of memory cartridges coupled to the system board and configured to store data figure 1 element 14;

a plurality of cartridge connectors coupled to the memory system board, each of the plurality of cartridge connectors configured to receive one of the plurality of memory cartridges and further configured to facilitate the insertion and removal of the memory cartridges while the system is powered-up in figure 1 element 16; and

Olarig however does not disclose the memory subsystem and host controller configured to facilitate the transition of the memory sub-system from the redundant mode of operation to the non-redundant mode of operation, and further configured to facilitate the transition of the memory sub-system from the non-redundant mode of operation to the redundant mode of operation. Santeler discloses RAID methods in memory (a redundant memory) in figures 4-6 when all memory banks are operating correctly the system is in a redundant mode, when a bank fails the system is in a non-redundant mode, upon replacement of the failed part the memory controller transitions the system back to a redundant mode as disclosed in column 2 lines 32-37. Santeler discloses the benefits of incorporating his invention with hot swap memory modules in column 2 lines 24 – 28. Likewise Olarig discloses the benefits of incorporating of redundant memory in column 14 lines 53-59. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate hot swappable memory with redundant memory banks for the purpose of maintaining data integrity and restoring the memory system without loss of data due to memory cartridge failure.

In regards to claim 17, Olarig discloses the host controller comprises error detection logic configured to detect errors in the data stored in the memory cartridges in column 14 lines 36-46.

In regards to claim 18, Olarig discloses the host controller comprises a plurality of drivers configured to drive the plurality of control logic devices in column 10 line 62 – column 11 line 5.

In regards to claim 19, Olarig discloses the indicator comprises a plurality of light devices, each of the plurality of light devices coupled to a light emitting diode and configured to illuminate in response to error detection in column 7 lines 23-28.

In regards to claim 25, Santeler discloses the memory sub-system comprises five memory cartridges in figure 5.

In regards to claim 26, while neither Santeler nor Olarig discloses each of the plurality of memory cartridges comprises a memory control device configured to control access to one of the plurality of memory cartridges, Olarig discloses in figure 2 a memory controller configured to control access to one of the plurality of memory cartridges. Changing the location of the memory controller onto the memory cartridge is an obvious modification that does not change the functionality of the system and

therefore would have been obvious to one having ordinary skill in the art at the time the invention was made to change the location of the memory controller.

In regards to claim 27, Olarig discloses each of the memory control devices comprises error detection logic configured to detect errors in the data stored in the plurality of memory cartridges in column 14 lines 37-46.

In regards to claim 29, Olarig discloses each of the plurality of light devices is associate with one of a memory cartridge and a DIMM in column 14 lines 37-46.

In regards to claim 30, Olarig discloses the plurality of control logic devices coupled to the memory system board, the plurality of control logic devices comprising:

a first device programmed to facilitate the exchange of a first set of control signals between the host controller and the memory sub-system in figure 12 element 341;

a plurality of power control devices coupled to the first device and configured to provide power fault detection in the computer system figure 2 element 44; and

a plurality of second devices coupled between the memory control device and the host controller and programmed to exchange a second set of control signals there between in figure 2 element 12.

In regards to claim 32, neither Olarig nor Santeler explicitly discloses the first device is a programmable array logic (PAL) device, however it is well known in the art the use of PAL to implement logic circuits of medium complexity, PAL's provide a smaller footprint than discreet Integrated Circuits (IC's) and is cheaper than a corresponding application specific IC (ASIC). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a PAL for the first device for the purpose of reducing the cost and footprint of the logic circuit.

In regards to claim 37, neither Olarig nor Santeler explicitly discloses the second device is a programmable array logic (PAL) device, however it is well known in the art the use of PAL to implement logic circuits of medium complexity, PAL's provide a smaller footprint than discreet Integrated Circuits (IC's) and is cheaper than a corresponding application specific IC (ASIC). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a PAL for the second device for the purpose of reducing the cost and footprint of the logic circuit.

In regards to claims 38, Olarig discloses the second set of control signals comprises a plurality of interrupt signals and a plurality of miscellaneous control signals in column 14 lines 47-59 and figure 5 elements 51, 53, CSOLC_O, CLK_IN, CLK_OUT, CSIL_O, CRERR, UCERR.

Claims 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. US Patent 6,098,132 in view of Santeler et al. US Patent 6,223,301 in further view of Windsor et al EP 398,188.

In regards to claim 20, neither Olarig nor Santeler explicitly discloses each of the plurality of memory cartridges comprises a plurality of memory modules. Windsor discloses the memory cartridge comprises a plurality of memory modules in figure 5b elements 300 and 400. Windsor discloses the use of memory cartridges to expand the memory of the memory subsystem, while Windsor's invention is concerned with older technologies of expanding memory it demonstrates that populating memory cartridges with a plurality of memory modules is well known in the art. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the plurality of memory cartridges comprised of a plurality of memory modules.

In regards to claim 21, While Windsor does not explicitly disclose the plurality of memory cartridges comprises four memory modules, in figures 5a and 5b it is possible to partially populate the board, since 4 memory modules is a possible combination (as he states in the abstract 1mb modules in 2mb increments ie 2,4,... modules)

In regards to claim 22, Santeler discloses each of the plurality of memory modules comprises a Dual Inline Memory Module (DIMM) in column 2 lines 35-39.

In regards to claims 23, Santeler discloses each of the plurality of memory modules comprises a plurality of memory devices configured to store data in figure 5.

In regards to claim 24, Olarig discloses each of the plurality of memory devices comprises a Synchronous Dynamic Random Access Memory (SDRAM) device in column 8 lines 45-49.

Claim 28 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. US Patent 6,098,132 in view of Santeler et al. US Patent 6,223,301 in further view of Liencres et al., JP 9,222,940.

In regards to claim 28, Neither Olarig nor Santeler discloses the pins being of varying lengths. Liencres discloses pins of varying lengths in Figure 3, the use of pins of varied (staggered) length is common practice in the art of hot insertion/removal of computer components as disclosed by Liencres. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to vary the pin length of the memory cartridge for the purpose of facilitating and orderly power up/ power down of the memory cartridge.

In regards to claim 31, Olarig does not disclose providing an audio alarm for the memory sub-system, the alarm being activated in the event of an illegal memory cartridge removal. Liencres discloses the use of an alarm to warn of improper removal

in figure 3 element 3120. Liencres' invention is concerned with proper removal and insertion of hot plug cards in a computer system. Since Liencres is in the identical field as Olarig and Santeler it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate an alarm in memory subsystem for the purpose of alerting the user about an improper removal.

Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. US Patent 6,098,132 in view of Santeler et al. US Patent 6,223,301 in further view of Bailis et al. US Patent 6,434,652.

In regards to claim 33, Neither Olarig nor Santeler explicitly discloses the first set of control signals comprise Present Detect signals, Power Fault signals, and Pre-Insertion Removal Notification Cable signals. Bailis discloses in figure 4 a present detect signal (signal Card Present (I)), a power fault signal (signal Card Power Good (G)), and a Pre-Insertion Removal Notification signal (signal Switch State (L)). Bailis is in the art hot plugging devices in computer systems. The handshaking signals presented in Bailis are an obvious addition to Olarig and Santeler to facilitate orderly powering up/down of the memory modules. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include Present Detect signals, Power Fault signals, and Pre-Insertion Removal Notification Cable signals for the purpose of orderly powering up/down memory modules.

In regards to claim 34, Neither Olarig nor Santeler explicitly discloses soft starting the memory module, Balis discloses ramping the voltage of the inserted module in column 5 lines 15-21. Bailis is in the art hot plugging devices in computer systems. The soft starting presented in Bailis are an obvious addition to Olarig and Santeler to facilitate orderly powering up/down of the memory modules. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the soft starting the memory module for the purpose of orderly powering up/down memory modules.

Claims 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. US Patent 6,098,132 in view of Santeler et al. US Patent 6,223,301 in further view of Rasums et al. US Patent 5,572,395.

In regards to claim 35, Neither Olarig nor Santeler disclose each of the plurality of power control devices is configured to provide over-current protection for the memory cartridge. Rasums discloses providing over-current protection for hot plug connections in column 3 lines 47-54. Ramsus states the need to for preventing over-current conditions in column 1 lines 35-53. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate over-current protection into the hot-plug system for the purpose of reducing risk of damage to memory cartridges.

In regards to claim 36, Neither Olarig nor Santeler disclose each of the plurality of power control devices is configured to provide under-voltage protection for the memory cartridge. Ramsus discloses providing under-voltage protection for hot-plug connections in column 3 lines 54-61. It is well known in the art that operating memory in under-voltage conditions leads to memory loss or corruption. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate under-voltage protection into the hot-plug memory system for the purpose of protecting data contained on the memory modules.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (703)305-3304. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703)306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PB

9/30/04

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER